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**1. Overview of complementary GaAs technology for high-speed VLSI circuits**

Brown, R.B.; Bernhardt, B.; LaMacchia, M.; Abrokwhah, J.; Parakh, P.N.; Basso, T.D.; G Stetson, S.; Gauthier, C.R.; Foster, D.; Crawford, B.; McQuire, T.; Sakallah, K.; Lomax T.N.;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on Volume 6, Issue 1, March 1998 Page(s):47 - 51

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Rousso, P.; Lew, P.; Gauthier, R.; Petrescu, D.; Cobo, J.; Vermette, Y.; Telecommunications Energy Conference, 1988. INTELEC '88., 10th International 30 Oct.-2 Nov. 1988 Page(s):257 - 264

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Herrell, D.J.; Beker, B.;
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1 [Low power converter circuits: Feasibility of monolithic and 3D-stacked DC-DC converters for microprocessors in 90nm technology generation](#)

Gerhard Schrom, Peter Hazucha, Jae-Hong Hahn, Volkan Kursun, Donald Gardner, Siva Narendra, Tanay Karnik, Vivek De

 August 2004 **Proceedings of the 2004 international symposium on Low power electronics and design**

 Full text available: [pdf\(225.30 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Rapidly increasing input current of microprocessors resulted in rising cost and motherboard real estate occupied by decoupling capacitors and power routing. We show by analysis that an on-die switching DC-DC converter is feasible for future microprocessor power delivery. The DC-DC converter can be fabricated in an existing CMOS process (90nm-180nm) with a back-end thin-film inductor module. We show that 85% efficiency and 10% output voltage droop can be achieved for 4:1, 3:1, and 2:1 conversion ...

Keywords: 3-D integration, DC-DC converter, integrated magnetics, on-die switching converter, power delivery

2 [Session 10C: Embedded tutorial: IC power distribution challenges: IC power distribution challenges](#)

Sudhakar Bobba, Tyler Thorp, Kathirgamar Aingaran, Dean Liu

 November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**


 Full text available: [pdf\(125.96 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

With each technology generation, delivering a timevarying current with reduced nominal supply voltage variation is becoming more difficult due to increasing current and power requirements. The power delivery network design becomes much more complex and requires accurate analysis and optimizations at all levels of abstraction in order to meet the specifications. In this paper, we describe techniques for estimation of the supply voltage variations that can be used in the design of the power delive ...

3 [Future performance challenges in nanometer design](#)

Dennis Sylvester, Himanshu Kaul

 June 2001 **Proceedings of the 38th conference on Design automation**

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We highlight several fundamental challenges to designing high-performance integrated circuits in nanometer-scale technologies (i.e. draRita Glover, EDA Today, L.C.wn feature sizes < 100 nm). Dynamic power scaling trends lead to major packaging problems. To alleviate these concerns, tMarc Halpernhermal monitoring and feedback mechanisms can limit worst-case dissipation and reduce costs. Furthermore, a flexible multi-Vdd + multi-Vth + re-sizing approach is advocated to leverage the inherent pr ...

4 [Proceedings of the SIGNUM conference on the programming environment for development of numerical software](#)

March 1979 **ACM SIGNUM Newsletter**, Volume 14 Issue 1

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5 [Power grid design and analysis techniques: A stochastic approach To power grid analysis](#)

Sanjay Pant, David Blaauw, Vladimir Zolotov, Savithri Sundareswaran, Rajendran Panda
June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available:  [pdf\(312.28 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Power supply integrity analysis is critical in modern high performance designs. In this paper, we propose a stochastic approach to obtain statistical information about the collective IR and Ldi/dt drop in a power supply network. The currents drawn from the power grid by the blocks in a design are modelled as stochastic processes and their statistical information is extracted, including correlation information between blocks in both space and time. We then propose a method to propagate the stat ...

Keywords: IR drop, Ldi/dt, power supply networks

6 [Power distribution issues: Macro-modeling concepts for the chip electrical interface](#)

Brian W. Amick, Claude R. Gauthier, Dean Liu

June 2002 **Proceedings of the 39th conference on Design automation**

Full text available:  [pdf\(515.95 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The power delivery network is made up of passive elements in the distribution network, as well as the active transistor loads. A chip typically has three types of power supplies that require attention: core, I/O, and analog. Core circuits consist of digital circuits and have the largest current demand. In addition to all of the system issues/models for the core, modeling the I/O subsystem has the additional requirement of modeling return paths and discontinuities. The analog circuits present yet ...

Keywords: VLSI power distribution, analog and I/O power delivery, high speed microprocessor design, inductance

7 [PixelFlow: the realization](#)

John Eyles, Steven Molnar, John Poulton, Trey Greer, Anselmo Lastra, Nick England, Lee Westover

August 1997 **Proceedings of the ACM SIGGRAPH/EUROGRAPHICS workshop on Graphics hardware**

Full text available:  [pdf\(1.54 MB\)](#) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)

Keywords: compositing, deferred shading, object-parallel, rendering, scalable

8 Power, buffering and open source: A fast algorithm for power grid design

Jaskirat Singh, Sachin S. Sapatnekar

April 2005 **Proceedings of the 2005 international symposium on physical design**

Full text available:  [pdf\(232.25 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This paper presents an efficient heuristic algorithm to design a power distribution network of a chip by employing a successive partitioning and grid refinement scheme. In an iterative procedure, the chip area is recursively bipartitioned, and the wire pitches and the wire widths of the power grid in the partitions are repeatedly adjusted to meet the voltage drop and current density specifications. By using the macromodels of the power grid constructed in the previous levels of partitioning, the ...

Keywords: bipartitioning, locality, macromodel, optimization, power grid design, wire pitch

9 Energy and thermal-aware design: Compact thermal modeling for temperature-aware design

Wei Huang, Mircea R. Stan, Kevin Skadron, Karthik Sankaranarayanan, Shougata Ghosh, Sivakumar Velusam

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available:  [pdf\(341.85 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)


Thermal design in sub-100nm technologies is one of the major challenges to the CAD community. In this paper, we first introduce the idea of *temperature-aware* design. We then propose a compact thermal model which can be integrated with modern CAD tools to achieve a temperature-aware design methodology. Finally, we use the compact thermal model in a case study of microprocessor design to show the importance of using temperature as a guideline for the design. Results from our thermal model s ...

Keywords: leakage, power-aware design, reliability, temperature-aware computing, temperature-aware design, thermal model

10 Power Grid and Signal Integrity Analysis: Scaling trends of on-chip Power distribution noise

Andrey V. Mezhiba, Eby G. Friedman

April 2002 **Proceedings of the 2002 international workshop on System-level interconnect prediction**

Full text available:  [pdf\(110.79 KB\)](#) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

The design of power distribution networks in high performance integrated circuits has become significantly more challenging with recent advances in process technology. As on-chip currents exceed tens of amperes and circuit clock periods are reduced well below a nanosecond, the signal integrity of the on-chip power supply has become a primary concern in integrated circuit design. The existing work on power distribution noise scaling is reviewed and extended to include the scaling of the inductanc ...

Keywords: power distribution, power supply noise, technology scaling

**11 System-level power optimization: techniques and tools**

Luca Benini, Giovanni de Micheli

April 2000 **ACM Transactions on Design Automation of Electronic Systems (TODAES)**,
Volume 5 Issue 2

Full text available: pdf(385.22 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

This tutorial surveys design methods for energy-efficient system-level design. We consider electronic systems consisting of a hardware platform and software layers. We consider the three major constituents of hardware that consume energy, namely computation, communication, and storage units, and we review methods of reducing their energy consumption. We also study models for analyzing the energy cost of software, and methods for energy-efficient software design and compilation. This survey ...

**12 On the impact of on-chip inductance on signal nets under the influence of power grid noise**

T. Chen

March 2001 **Proceedings of the conference on Design, automation and test in Europe**

Full text available: pdf(5.04 MB)

Additional Information: [full citation](#), [references](#), [index terms](#)**13 Power grid design and analysis techniques: Optimal placement of power supply pads and pins**

Min Zhao, Yuhong Fu, Vladimir Zolotov, Savithri Sundareswaran, Rajendran Panda

June 2004 **Proceedings of the 41st annual conference on Design automation**

Full text available: pdf(207.21 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

Power delivery networks of VLSI chips require adequate input supply connections to ensure reliable performance. This paper addresses the problem of finding an optimum set of pads, pins, and on-chip voltage regulators, and their placement in a given power supply network, subject to constraints on the voltage drops in the network and maximum currents through the pads, pins and regulators. The problem is modeled as a mixed integer linear program using macromodeling techniques and several heuristic ...

Keywords: pad optimization, pad placement**14 Low Power Design: Power and CAD considerations for the 1.75mbyte, 1.2ghz L2 cache on the alpha 21364 CPU**

Joel Grodstein, Rachid Rayess, Tad Truex, Linda Shattuck, Sue Lowell, Dan Bailey, David Bertucci, Gabriel Bischoff, Daniel Dever, Mike Gowan, Roy Lane, Brian Lilly, Krishna Nagalla, Rahul Shah, Emily Shriver, Shi-Huang Yin, Shannon Morton


April 2002 **Proceedings of the 12th ACM Great Lakes symposium on VLSI**

Full text available: pdf(205.76 KB)

Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

A 1.75 MByte L2 cache has been designed and fabricated as part of the Alpha 21364 microprocessor[1] (Figure 1), in a .18m bulk CMOS process. The cache was designed to run at 1.2 GHz, and pass-1 samples confirm this. While Alpha CPUs are known primarily for high speed, the combination of package constraints and a tight schedule forced careful attention to the integrated whole of power expenditure and the interaction of CAD with design. The cache consumes only 7% of total die power.

Keywords: CPU, cache memory, logic verification, low-power, timing verification

15 On-chip inductance modelingDavid Blaauw, Kaushik Gala, Vladimir Zolotov, Rajendran Panda, Junfeng Wang
March 2000 **Proceedings of the 10th Great Lakes symposium on VLSI**Full text available:  pdf(576.07 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

With operating frequencies approaching the gigahertz range, inductance is becoming an increasingly important consideration in the design and analysis of on-chip interconnect. We present an accurate technique for modeling and analyzing the effects of parasitic inductance on power grid noise, signal delay and crosstalk. We propose a detailed circuit model composed of interconnect resistance, inductance and distributed capacitance, device decoupling capacitances, quiescent activity in the grid, ...

16 Challenges and design choices in nanoscale CMOSSiva G. Narendra
March 2005 **ACM Journal on Emerging Technologies in Computing Systems (JETC)**,
Volume 1 Issue 1Full text available:  pdf(5.35 MB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

The driving force for the semiconductor industry growth has been the elegant scaling nature of CMOS technology. In this article, we will first review the history of technology scaling that follows Moore's law from the perspective of microprocessor designs. Challenges to continue the historical scaling trends will be highlighted and design choices to address two specific challenges, process variation and leakage power, will be discussed. In nanoscale CMOS technology generations, supply and thresh ...

Keywords: CMOS, leakage power, nanoscale, process variation

17 Getting to the bottom of deep submicron II: a global wiring paradigmDennis Sylvester, Kurt Keutzer
April 1999 **Proceedings of the 1999 international symposium on Physical design**Full text available:  pdf(1.23 MB) Additional Information: [full citation](#), [references](#), [citations](#), [index terms](#)**18** Session 10C: Embedded tutorial: IC power distribution challenges: Challenges in power-ground integrityShen Lin, Norman Chang
November 2001 **Proceedings of the 2001 IEEE/ACM international conference on Computer-aided design**Full text available:  pdf(54.74 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [citations](#), [index terms](#)

With the advance of semiconductor manufacturing, EDA, and VLSI design technologies, circuits with increasingly higher speed are being integrated at an increasingly higher density. This trend causes correspondingly larger voltage fluctuations in the on-chip power distribution network due to IR-drop, $L di/dt$ noise, or LC resonance. Therefore, Power-Ground integrity becomes a serious challenge in designing future high-performance circuits. In this paper, we will introduce Power-Ground integrity, ad ...

19 Power grid design and analysis techniques: Efficient power/ground network analysis for power integrity-driven design methodologySu-Wei Wu, Yao-Wen Chang
June 2004 **Proceedings of the 41st annual conference on Design automation**Full text available:  pdf(177.31 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

As technology advances, the metal width is decreasing with the length increasing, making the resistance along the power line increase substantially. Together with the nonlinear scaling of the threshold voltage that makes the ratio of the threshold voltage to the supply voltage rise, the voltage (IR) drop become a serious problem in modern VLSI design. Traditional power/ground (P/G) network analysis methods are typically very computationally expensive and thus not feasible to be integrated into f ...

Keywords: footnotesize floorplanning, power/ground network

20 Highlights of ISSCC and the design of state-of-the-art microprocessors: A 1.5GHz third generation itanium® 2 processor

Jason Stinson, Stefan Rusu

June 2003 **Proceedings of the 40th conference on Design automation**

Full text available:  pdf(403.60 KB) Additional Information: [full citation](#), [abstract](#), [references](#), [index terms](#)

This 130nm Itanium® 2 processor implements the Explicitly Parallel Instruction Computing (EPIC) architecture and features an on-die 6MB, 24-way set associative L3 cache. The 374mm² die contains 410M transistors and is implemented in a dual-Vt process with 6 layers copper interconnect and FSG dielectric. The processor runs at 1.5GHz at 1.3V and dissipates a maximum of 130W. This paper reviews circuit design and package details, power delivery, RAS, DFT and DFM features, as well as an overvie ...

Keywords: design methodology, on-die cache, processor, reliability, test

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NAME	CITY	STATE	COUNTRY	RULE-47
<u>Gauthier</u> , Claude R.	Fremont	CA	US	
Amick, Brian W.	Sunnyvale	CA	US	

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